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REMARKS

This Amendment seeks to place this application in condition for allowance. All of the Examiner's rejections have been addressed. Several of the pending claims have been amended. New dependent claims 189-192 have been added to more fully claim Applicants' invention. No new matter has been added.

OFFICE ACTION

In the Office Action mailed November 6, 2001, claims 151-188 have been rejected under 35 USC 112. In this regard, the Examiner stated: "[i]n claims 151-188, it is not clear what the first operation code is, and how the first operation code is sampled."

Applicants submit that the "operation code(s)" is control information that specifies the type of access of the device, for example, control information that initiates a read operation in the memory device (e.g., as in claim 151), control information that initiates a write operation in the memory device[1] (e.g., as in claim 159), or control information that initiates an access of a programmable register[2] (e.g., as in claim 164). Where the "operation code(s)" initiates an access of a programmable register in the memory device (e.g., as in claim 164) in order to store data in the register, the memory device responds to the operation code

1 The specification, on page 22, line 22 to page 23 line 3, recites "In a preferred implementation, AccessType[0] is a Read/Write switch: if it is a 1, then the operation calls for a read from the slave (the slave to read the requested memory block and drive the memory contents onto the bus); if it is a 0, the operation calls for a write into the slave (the slave to read data from the bus and write it to memory)."

2 The specification, on page 22, lines 19-21, recites "The AccessType field specifies whether the requested operation is a read or write and the type of access, for example, whether it is to control registers..."

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by storing the data (e.g., a binary value) in the register;[3] where the operation code initiates a read operation, the memory device outputs data accessed from the memory array; and where the operation code initiates a write operation, the memory device inputs data to be written to the memory array.

The specification describes several embodiments in which semiconductor device(s) (e.g., semiconductor memory devices) include "a set of internal registers, preferably including a device identification (device ID) register, a device-type descriptor register, control registers and other registers containing other information relevant to that type of device." (see page 14, lines 3-7). IN one embodiment, several of these registers (e.g., the address registers) are programmed in response to an operation code. (see page 23, lines 12-21; see also, page 14, lines 13-21; and page 35, line 23 to page 36, line 1).

In one embodiment, the operation code is "AccessType[0:3]" (see page 22, lines 12-13). One type of access is, for example, writing a binary value that represents control data into a programmable register. ("The AccessType field specifies ... the type of access, for example, whether it is to control registers ...." (see page 22, lines 19-21)).

When the operation code initiates an access to the register in order to store data in the register, the memory device responds by

3 It should be noted that certain dependent claims add further limitations to the operation code, for example, the operation code is included in a request packet (e.g., claim 160); the operation code is sampled synchronously with respect to a transition of the external clock signal (e.g., claim 173); and the binary value and the operation code are multiplexed over a plurality of signal lines (e.g., as in claim 184).

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storing the data (i.e., the value) in the register. In this regard, the specification states:

> One special type of access is control register access, which involves addressing a selected register in a selected slave. In the preferred implementation of this invention, AccessType [1:3] equal to zero indicates a control register request and the address field of the packet indicates the desired control register. For example... the least significant three bytes can specify a register address and may also represent or include data to be loaded into that control register. (page 23, lines 12-21)

Input receivers within the memory device sample the operation code (e.g., AccessType[0:3]). (see, e.g., page 53, lines 6-8; page 53, line 24 to page 54, line 7; and Figure 10). In one embodiment, the operation code is sampled synchronously with respect to an external clock signal. (see, page 54, lines 3-8; see also, page 46, line 23 to page 47, line 1). In a preferred embodiment, the operation code is sampled synchronously with respect to complementary internal device clocks. (e.g., internal device clocks 73 and 74 in Figures 10 and 13; see page 58 lines 18-21). The internal device clocks are generated within the memory device using an external clock. (see, page 57, lines 3-25, page 58, lines 16-21 and Figure 13; see also, page 46, line 23 to page 47, line 1). Here, the internal device clocks are synchronized with edge transitions of the external clock (e.g., a rising edge transition). (see, page 58, lines 1-18 and Figure 13).

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Information Disclosure Statement

Submitted concurrently herewith by first class mail is an Information Disclosure Statement ("IDS"), including a modified Form PTO-1449, and a copy of all of the documents listed on the PTO-1449. It should be noted that the documents listed on the PTO-1449 were referenced in a communication from the Japanese Patent Office (hereinafter "COMMUNICATION") in a Japanese application that claims priority to U.S. Application Serial No. 07/510,898 -- a parent of the instant application. A copy of the IDS and modified Form PTO-1449 is enclosed herewith. It is respectfully requested that the Examiner make his consideration of these references formally of record with the next action.

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Conclusion

Applicants request reconsideration of the instant application and entry of the foregoing amendments. Applicants submit that the pending claims present patentable subject matter. Accordingly, allowance of all of the claims is respectfully requested.

Respectfully submitted,

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Exhibit A -- Version with Markings to Show Changes Made

154. (Amended) The method of claim 151 wherein the delay time is representative of a number of clock cycles of the external clock signal [to transpire].

158. (Amended) The method of claim 151 further including:

receiving block size information, wherein the block size information is representative of an amount of data to be output;

receiving the second operation code; and

outputting the amount of data in response to the second operation code, after the delay time transpires.

160. (Amended) The method of claim 159 wherein the third operation code is included in a write request packet.

161. (Amended) The method of claim 160 wherein the block size information and the third operation code are included in the same write request packet.

167. (Amended) The method of claim 166 further including providing address information to the memory device synchronously with respect to the external clock signal.

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169. (Amended) The method of claim 164 further including:

providing block size information to the memory device, wherein the block size information defines an amount of data to be output by the memory device in response to a[the] second operation code;

issuing the second operation code to the memory device; and

receiving the amount of data output by the memory device.

173. (Twice Amended) A synchronous memory device including an array of memory cells, the synchronous memory device [comprises] comprising:

a clock receiver [circuitry] to receive an external clock signal;

a plurality of input receivers [circuitry] to sample a first operation code synchronously with respect to a transition of the external clock signal; and

a programmable register to store a binary value, wherein the memory device stores the binary value in the programmable register in response to the first operation code.

175. (Twice Amended) The memory device of claim 174 further including a plurality of output drivers [circuitry] to output the data, after the number of clock cycles of the external clock signal transpire, in response to the second operation code.

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176. (Twice Amended) The memory device of claim [175] 173 further including a plurality of output drivers to output data, wherein the data is output in response to a second operation code that initiates a read operation, and wherein the plurality of output drivers [circuitry] output[s] a first portion of the data synchronously with respect to a rising edge transition of the external clock signal and output a second portion of the data synchronously with respect to a falling edge transition of the external clock signal.

179. (Amended) The memory device of claim 178 [173] wherein the first operation code and the binary value are included in the same request packet.

180. (Amended) The memory device of claim 173 wherein the plurality of input receivers [circuitry is] are operative to receive a [third] second operation code, wherein the [third] second operation code initiates a write operation in the memory device, and wherein the memory device further includes:

input receivers [circuitry] to input data in response to the [third] second operation code.

182. (Amended) The method of claim 181 wherein the external bus includes a plurality of signal lines, and wherein the binary value and the first operation code are multiplexed over the plurality of signal lines.

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184. (Amended) The method of claim 183 wherein the external bus includes a plurality of signal lines, and wherein the binary value and the first operation code are multiplexed over the plurality of signal lines.

186. (Amended) The memory device of claim 173 wherein the plurality of input receivers [circuitry] sample[s] the first operation code from an external bus.

187. (Amended) The memory device of claim 186 wherein the external bus includes a plurality of signal lines, and wherein the first operation code and the binary value [address information] are multiplexed over the plurality of signal lines.

188. (Amended) The memory device of claim 187 wherein data, the first operation code and the binary value[address information] are multiplexed over the plurality of signal lines.